Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method for forming an isolation layer of a semiconductor device, comprising:

providing a silicon substrate in which an active region and a field region are defined;

forming a trench in ~~the silicon substrate within~~ the field region;

forming an insulating layer ~~to be used as the isolation layer~~ on the silicon substrate ~~including the trench~~, thereby filling the trench with the insulating layer;

forming a capping layer on a resultant entire structure including the insulating layers;

~~selectively removing~~ etching the capping layer to expose an upper portion of the insulating layer within the active region;

removing the upper portion of the ~~exposed~~ insulating layer ~~with the active region~~; and

removing [[the]] a residual portion of the capping layer~~, so that the isolation layer is obtained from the insulating layer remaining in the trench~~.

2. (Original) The method of claim 1, wherein the insulating layer has a first portion filled in the trench within the field region and a second portion formed on the silicon substrate within the active region, and wherein the first portion is physically separated from the second portion.

3. (Original) The method of claim 1, wherein the insulating layer includes a high density plasma undoped silicate glass (HDP-USG) layer.

4. (Original) The method of claim 1, wherein the capping layer includes a nitride layer.

5. (Currently Amended) The method of claim 1, wherein the etching ~~selectively removing~~ of the capping layer uses a reverse photo mask.

6. (Currently Amended) The method of claim 1, wherein the removing of the ~~exposed~~ upper portion of the insulating layer and the removing of the residual portion of the capping layer [[use]] respectively use wet etching process.

7. (Currently Amended) A method for forming an isolation layer of a semiconductor device, comprising:

providing a silicon substrate having an active region and a field region;

sequentially forming a pad oxide layer and a silicon nitride layer on the silicon substrate;

forming a trench in the silicon substrate to define the field region by selectively removing the silicon nitride layer, the pad oxide layer and an upper portion of the silicon substrate;

forming an insulating layer to be used as the isolation layer on the silicon nitride layer and the trench, thereby filling the trench with the insulating layer;

forming a capping layer on a resultant entire structure including the insulating layer;

~~selectively removing~~ etching the capping layer to expose an upper portion of the insulating layer within the active region;

removing the upper portion of the insulating layer ~~exposed insulating layer within the active region~~;

removing [[the]] a residual portion of the capping layer and the silicon nitride layer; and

removing the pad oxide layer~~, so that the isolation layer is obtained from the insulating layer remaining in the trench~~.

8. (Original) The method of claim 7, wherein the insulating layer has a first portion filled in the trench within the field region and a second portion formed on the silicon nitride layer within the active region, and wherein the first portion is physically separated from the second portion.

9. (Original) The method of claim 7, wherein the insulating layer includes a high density plasma undoped silicate glass (HDP-USG) layer.

10. (Original) The method of claim 7, wherein the capping layer includes a nitride layer.

11. (Currently Amended) The method of claim 7, wherein the ~~selectively removing~~ etching of the capping layer uses a reverse photo mask.

12. (Currently Amended) The method of claim 7, wherein the removing of the upper portion of the insulating layer ~~exposed insulating layer~~ uses a first wet etching.

13. (Currently Amended) The method of claim 7, wherein the removing of the residual portion of the capping layer and the silicon nitride layer uses a second wet etching.

14. (Currently Amended) A method for forming a shallow trench isolation layer of a semiconductor device, comprising:

providing a silicon substrate having an active region and a field region;

sequentially forming a pad oxide layer and a silicon nitride layer on the silicon substrate;

forming a trench in the silicon substrate to define the field region by selectively removing the silicon nitride layer, the pad oxide layer and an upper portion of the silicon substrate;

forming a high density plasma undoped silicate glass (HDP-USG) layer to be used as the shallow trench isolation layer on the silicon nitride layer and the trench, thereby filling the trench with the HDP-USG layer;

forming a nitride layer on the resultant entire structure including the HDP-USG layer;

forming a reverse photo mask on the nitride layer to cover the field region and to expose the active region;

~~selectively removing~~ etching the nitride layer to expose an upper portion of the HDP-USG layer within the active region by using the reverse photo mask as an etch barrier;

removing the upper portion of the ~~exposed~~ HDP-USG layer within the active region by using a first wet etching after removing the reverse photo mask;

removing [[the]] a residual portion of the nitride layer and the silicon nitride layer by using a second wet etching; and

removing the pad oxide layer, so that the shallow trench isolation layer is obtained from the HDP-USG layer remaining in the trench.

15. (Original) The method of claim 14, wherein the HDP-USG layer has a first portion filled in the trench within the field region and a second portion formed on the silicon nitride layer within the active region, and wherein the first portion is physically separated from the second portion.